IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application : 10/076,374

Applicant(s) : van der SCHAAR

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Examiner : CZEKAJ, David J.

Atty. Docket : US-020044

Title: MEMORY-BANDWIDTH EFFICIENT FGS ENCODER

Mail Stop: APPEAL BRIEF - PATENTS
Commissioner for Patents
Alexandria, VA 22313-1450

APPEAL UNDER 37 CFR 41.37

Sir:

This is an appeal from the decision of the Examiner dated 25 August 2006, finally rejecting claims 21-40 of the subject application.

This paper includes (each beginning on a separate sheet):

1. Appeal Brief;
2. Claims Appendix;
3. Evidence Appendix; and
4. Related Proceedings Appendix.

APPEAL BRIEF

I. REAL PARTY IN INTEREST

The above-identified application is assigned, in its entirety, to **Koninklijke Philips Electronics N. V.**

II. RELATED APPEALS AND INTERFERENCES

Appellant is not aware of any co-pending appeal or interference that will directly affect, or be directly affected by, or have any bearing on, the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-20 are canceled.

Claims 21-40 are pending in the application.

Claims 38-40 stand rejected by the Examiner under 35 U.S.C. 101.

Claims 21-40 stand rejected by the Examiner under 35 U.S.C. 103(a).

These rejected claims are the subject of this appeal.

IV. STATUS OF AMENDMENTS

No amendments were filed subsequent to the final rejection in the Office Action dated 25 August 2006.

V. SUMMARY OF CLAIMED SUBJECT MATTER

This invention addresses video encoding using a progressive encoding scheme, such as fine granular scaling (page 9, line 28-page 10, line 2). In an example embodiment, each transform block (e.g. an 8x8 DCT block in MPEG (page 10, lines 3-6)) is bit-plane encoded and stored as it is received (page 5, lines 6-10), thereby avoiding the need to provide a frame memory for storing the DCT blocks prior to a frame-based bit-plane encoding as in conventional systems (page 5, lines

13-25). The bit-plane data is preferably stored in a sequential bit-plane order, thereby providing compatibility with conventional decoding systems (page 7, lines 26-30).

As claimed in independent claim 21, an embodiment of the invention comprises a method (FIG. 6) that includes:

receiving (600) a plurality of transform blocks in a sequential transform-block order (page 6, lines 29-30),

converting (610-612) each of the plurality of transform blocks into a plurality of bit-plane encodings (page 7, lines 10-13),

storing (614) each of the plurality of bit-plane encodings in a sequential bit-plane order of a memory (page 7, lines 14-23) prior to converting (600) another of the plurality of transform blocks (page 6, lines 26-27), and

transmitting each bit-plane encoding of the plurality of transform blocks in the sequential bit-plane order (618) (page 7, line 26 – page 8, line 3).

As claimed in dependent claim 24, an embodiment of the invention includes the method of claim 21, wherein storing (614) each bit-plane encoding in the memory includes storing the bit-plane encoding for each subsequently received transform block in memory locations following the stored corresponding bit-plane encoding of a prior received transform block (page 7, lines 14-23).

As claimed in independent claim 29, an embodiment of the invention comprises an apparatus (FIG. 5) that includes:

a memory (558), and

a converter (504) (page 8, lines 8-9) that is configured to:

receive (550) a plurality of transform blocks in a sequential transform-block order (page 8, lines 22-24),

convert (553) each of the plurality of transform blocks into a plurality of bit-plane encodings (page 8, lines 25-31), and

store each of the plurality of bit-plane encodings in a sequential bit-plane order of the memory prior to converting another of the plurality of transform blocks (page 9, lines 1-6).

As claimed in independent claim 38, an embodiment of the invention comprises a computer readable medium that includes computer program code (page 10, lines 8-15), which, when executed on a processor, enables the processor to:

receive (page 6, lines 29-30) a plurality of transform blocks in a sequential transform-block order,

convert (page 7, lines 10-13) each of the plurality of transform blocks into a plurality of bit-plane encodings, and

store (page 7, lines 14-23) each of the plurality of bit-plane encodings in a sequential bit-plane order of a memory prior to converting another of the plurality of transform blocks (page 6, lines 26-27).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 38-40 stand rejected under 35 U.S.C. 101.

Claims 21-27, 29-32, 35-36, 38, and 40 stand rejected under 35 U.S.C. 103(a) over Wu et al. (USP 6,956,972, hereinafter Wu) and Chen et al. (USP 6,798,364, hereinafter Chen).

Claims 28 and 37 stand rejected under 35 U.S.C. 103(a) over Wu, Chen, and Lafe (USP 6,456,744).

Claims 33-34 and 39 stand rejected under 35 U.S.C. 103(a) over Wu, Chen, and Monro (WO 98/37700).

VII. ARGUMENT

Claims 38-40 stand rejected under 35 U.S.C. 101

Claims 38-40

The Office action asserts that a claim to a computer readable medium that includes computer program code must specifically use the term "encoded with" instead of "includes" (Office action, page 2, lines 14-16). The applicant respectfully disagrees with this assertion.

MPEP 2106 specifically provides guidance for evaluating computer-related inventions:

> "Office personnel have the burden to establish a *prima facie* case that the claimed invention as a whole is directed to solely an abstract idea or to manipulation of abstract ideas or does not produce a useful result. ***Only when the claim is devoid of any limitation to a practical application in the technological arts should it be rejected under 35 U.S.C. 101.*** Compare *Musgrave*, 431 F.2d at 893, 167 USPQ at 289; *In re Foster*, 438 F.2d 1011, 1013, 169 USPQ 99, 101 (CCPA 1971)...
> As the Supreme Court has held, Congress chose the expansive language of 35 U.S.C. 101 so as to include "***anything under the sun that is made by man***." *Diamond v. Chakrabarty*, 447 U.S. 303, 308-09, 206 USPQ 193, 197 (1980). Accordingly, section 101 of title 35, United States Code, provides:
> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Neither 35 U.S.C. 101 nor MPEP 2106 supports the Examiner's assertion that unless a specific term is used in a claim, the claim is rejectable under 35 U.S.C. 101.

Claims 21-27, 29-32, 35-36, 38, and 40 stand rejected under 35 U.S.C. 103(a) over Wu and Chen

MPEP 2142 states:

> "To establish a *prima facie* case of obviousness ... the prior art reference (or references when combined) ***must teach or suggest all the claim limitations***... If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness."

Claims 21-27

The combination of Wu and Chen fails to teach or suggest storing each of the plurality of bit-plane encodings in a sequential bit-plane order of a memory prior to converting another of the plurality of transform blocks, as specifically claimed in claim 21, upon which claims 22-28 depend.

The Office action fails to address the specific elements of this limitation. The Office action fails to address storing the encoding of each block's bit-plane encoding prior to converting another block. As noted at page 5, lines 6-25, performing this operation provides substantial advances over the prior art.

Wu specifically teaches that all of the blocks are transformed before the bit-plane encoding occurs. Chen does not address the transformation of blocks.

Wu's FIG. 9 illustrates a Frame Memory 222 that is configured to store the DCTs (Discrete Cosine Transforms) for a full frame; this Frame Memory 222 provides the input to bit-plane variable length encoders (VLC) 226(1)… 226(n-1). That is, Wu's bit level encoding is applied after an entire frame of a plurality of DCT blocks is processed, consistent with conventional MPEG processing as illustrated in the applicant's prior art figure FIG. 3.

Additionally, Wu specifically states that the contents of memory 222 are arranged in the conventional zig-zag order used to store DCT coefficients (Wu, column 9, lines 39-41), whereas the applicant specifically claims storing each of the plurality of bit-plane encodings in a sequential bit-plane order.

Chan teaches a technique for variable length encoding. Chan does not address the source of the data that is being variable length encoded, and specifically does not address the order in with the source data is created with respect to the processing of transform blocks.

Because the combination of Wu and Chan fails to teach or suggest storing each of the plurality of bit-plane encodings in a sequential bit-plane order of a memory prior to converting another of the plurality of transform blocks, as specifically claimed in claim 21, the applicant respectfully maintains that the rejection of claims 21-27 under 35 U.S.C. 103(a) over Wu and Chen is unfounded, per MPEP 2142.

Claim 24

The combination of Wu and Chen fails to teach storing the bit-plane encoding for each subsequently received transform block in memory locations following the stored corresponding bit-plane encoding of a prior received transform block, as specifically claimed in claim 24.

In support of this rejection, the Office action asserts that Chen provides this teaching at column 5, lines 33-36. As noted above, Chen does not address the source of the data to be variable-length encoded, and specifically does not address the order of storing the bit-plane encodings relative to transform blocks. The cited text follows:

> "The process repeats itself until the destination buffer has been filled with bits from the desired bit plane, or an alternative limit has been reached. For example, one embodiment may store two desired bit planes in a buffer." (Chen, column 5, lines 33-36)

As can be seen, the cited text fails to address storing a bit-plane encoding for each block at memory locations following the stored encodings of a prior transform block, and thus the Office action fails to identify where the combination of Wu and Chen teaches or suggests each limitation of claim 24.

Because the combination of Wu and Chen fails to teach storing the bit-plane encoding for each subsequently received transform block in memory locations following the stored corresponding bit-plane encoding of a prior received transform block, the applicant respectfully maintains that the rejection of claim 24 under 35 U.S.C. 103(a) over Wu and Chen is unfounded, per MPEP 2142.

Claims 29-32 and 35-36

The combination of Wu and Chen fails to teach or suggest a converter that stores each of a plurality of bit-plane encodings of a transform block in a sequential bit-plane order of a memory prior to converting another of transform block, as specifically claimed in claim 29, upon which claims 30-37 depend.

As noted above, the Office action does not address the limitation of storing each bit-plane encoding of a transform block prior to converting another transform block, and thus fails to establish a prima facie case of obviousness. As such, the applicant respectfully maintains that the rejection of claims 29-32 and 35-36 under 35 U.S.C. 103(a) over Wu and Chen is unfounded, per MPEP 2142.

Claims 38 and 40

The combination of Wu and Chen fails to teach or suggest computer program code that enables a processor to store each of a plurality of bit-plane encodings of a transform block in a sequential bit-plane order of a memory prior to converting another transform block, as specifically claimed in claim 38, upon which claims 39-40 depend.

As noted above, the Office action does not address the limitation of storing each bit-plane encoding of a transform block prior to converting another transform block, and thus fails to establish a prima facie case of obviousness. As such, the applicant respectfully maintains that the rejection of claims 29-32 and 35-36 under 35 U.S.C. 103(a) over Wu and Chen is unfounded, per MPEP 2142.

Claims 28 and 37 stand rejected under 35 U.S.C. 103(a) over Wu, Chen, and Lafe

Claim 28

Claim 28 is dependent upon claim 21. In this rejection, the Office action relies upon the combination of Wu and Chen for teaching the limitations of claim 21.

As noted above, the combination of Wu and Chen does not teach or suggest each of the limitations of claim 21. As such, the applicant respectfully maintains that the rejection of claim 28 under 35 U.S.C. 103(a) that relies on Wu and Chen for teaching the limitations of claim 21 is unfounded, per MPEP 2142.

Claim 37

Claim 37 is dependent upon claim 29. In this rejection, the Office action relies upon the combination of Wu and Chen for teaching the limitations of claim 29.

As noted above, the combination of Wu and Chen does not teach or suggest each of the limitations of claim 29. As such, the applicant respectfully maintains that the rejection of claim 37 under 35 U.S.C. 103(a) that relies on Wu and Chen for teaching the limitations of claim 29 is unfounded, per MPEP 2142.

Claims 33-34 and 39 stand rejected under 35 U.S.C. 103(a) over Wu, Chen, and Monro

Claims 33-34

Claims 33-34 are dependent upon claim 29. In this rejection, the Office action relies upon the combination of Wu and Chen for teaching the limitations of claim 29.

As noted above, the combination of Wu and Chen does not teach or suggest each of the limitations of claim 29. As such, the applicant respectfully maintains that the rejection of claims 33-24 under 35 U.S.C. 103(a) that relies on Wu and Chen for teaching the limitations of claim 29 is unfounded, per MPEP 2142.

Claim 39

Claim 39 is dependent upon claim 38. In this rejection, the Office action relies upon the combination of Wu and Chen for teaching the limitations of claim 38.

As noted above, the combination of Wu and Chen does not teach or suggest each of the limitations of claim 38. As such, the applicant respectfully maintains that the rejection of claim 39 under 35 U.S.C. 103(a) that relies on Wu and Chen for teaching the limitations of claim 38 is unfounded, per MPEP 2142.

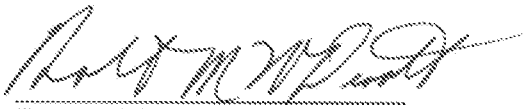
CONCLUSIONS

Because the use of "includes" instead of "encoded with" does not render a claim unpatentable, the applicant respectfully requests that the Examiner's rejection of claims 38-40 under 35 U.S.C. 101 be reversed by the Board, and the claims be allowed to pass to issue.

Because the combination of Wu and Chan fails to teach or suggest storing each of the plurality of bit-plane encodings of a transform block in a sequential bit-plane order of a memory prior to converting another of the plurality of transform blocks, as specifically claimed in each of the applicant's independent claims 21, 29, and 38, the applicant respectfully requests that the Examiner's rejection of claims 21-40 under 35 U.S.C. 103(a) be reversed by the Board, and the claims be allowed to pass to issue.

Because the combination of Wu and Chan fails to teach or suggest storing the bit-plane encoding for each subsequently received transform block in memory locations following the stored corresponding bit-plane encoding of a prior received transform block, the applicant respectfully requests that the Examiner's rejection of claim 24 under 35 U.S.C. 103(a) be reversed by the Board, and the claim be allowed to pass to issue.

Respectfully submitted



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CLAIMS APPENDIX

1-20 (Canceled)

21. A method comprising:

receiving a plurality of transform blocks in a sequential transform-block order,

converting each of the plurality of transform blocks into a plurality of bit-plane encodings,

storing each of the plurality of bit-plane encodings in a sequential bit-plane order of a memory prior to converting another of the plurality of transform blocks, and

transmitting each bit-plane encoding of the plurality of transform blocks in the sequential bit-plane order.

22. The method of claim 21, wherein the sequential bit-plane order is from most-significant bit to least-significant bit of transform coefficients in each transform block.

23. The method of claim 21, wherein the bit-plane encodings include a run-length encoding.

24. The method of claim 21, wherein storing each bit-plane encoding in the memory includes storing the bit-plane encoding for each subsequently received transform block in memory locations following the stored corresponding bit-plane encoding of a prior received transform block.

25. The method of claim 21, including

discarding each transform block after converting each of the bit-plane encodings for the transform block, and prior to transmitting a first bit-plane encoding of the plurality of transform blocks.

26. The method of claim 21, wherein each transform block corresponds to a residual image of a fine granular scalability (FGS) encoding.

27. The method of claim 21, wherein the transform blocks correspond to one of: a discrete cosine transform, a block-based wavelet transform, and a matching pursuit transform.

28. The method of claim 21, wherein converting each transform block includes identifying a maximum transform coefficient within the transform block, and determining the plurality of bit-plane encodings for the transform block based on the maximum transform coefficient.

29. An apparatus comprising:

a memory,

a converter that is configured to:

receive a plurality of transform blocks in a sequential transform-block order,

convert each of the plurality of transform blocks into a plurality of bit-plane encodings, and

store each of the plurality of bit-plane encodings in a sequential bit-plane order of the memory prior to converting another of the plurality of transform blocks.

30. The apparatus of claim 29, including

a transmitter that is configured to transmit each bit-plane encoding of the plurality of transform blocks in the sequential bit-plane order.

31. The apparatus of claim 29, wherein the sequential bit-plane order is from most-significant bit to least-significant bit of transform coefficients in each transform block.

32. The apparatus of claim 29, wherein the bit-plane encodings include a run-length encoding.

33. The apparatus of claim 29, wherein the converter is configured to:

store a first bit-plane encoding of a first transform block at a first location of the memory and a second bit-plane encoding of the first transform block at a second location of the memory, and

store a corresponding first bit-plane encoding of a second transform block at a third location that is between the first and second locations of the memory.

34. The apparatus of claim 33, wherein the third location is immediately adjacent the first location.

35. The apparatus of claim 29, wherein each transform block corresponds to a residual image of a fine granular scalability (FGS) encoding.

36. The apparatus of claim 29, wherein the transform blocks correspond to one of: a discrete cosine transform, a block-based wavelet transform, and a matching pursuit transform.

37. The apparatus of claim 29, wherein the converter is configured to:

determine a maximum transform coefficient within the transform block, and

determine the plurality of bit-plane encodings for the transform block based on the maximum transform coefficient.

38. A computer readable medium that includes computer program code, which, when executed on a processor, enables the processor to:

receive a plurality of transform blocks in a sequential transform-block order,

convert each of the plurality of transform blocks into a plurality of bit-plane encodings, and

store each of the plurality of bit-plane encodings in a sequential bit-plane order of a memory prior to converting another of the plurality of transform blocks.

39. The computer readable medium of claim 38, wherein the processor is enabled to:

store a first bit-plane encoding of a first transform block at a first location of the memory and a second bit-plane encoding of the first transform block at a second location of the memory, and

store a corresponding first bit-plane encoding of a second transform block at a third location that is between the first and second locations of the memory.

40. The computer readable medium of claim 38, wherein the bit-plane encodings include a run-length encoding.

EVIDENCE APPENDIX

No evidence has been submitted that is relied upon by the appellant in this appeal.

RELATED PROCEEDINGS APPENDIX

Appellant is not aware of any co-pending appeal or interference which will directly affect or be directly affected by or have any bearing on the Board's decision in the pending appeal.